

In the Claims:

Please amend claims 1-2, 5-9 and 12-15 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A frame synchronizing device for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, the device comprising:
a serial input parallel output shift register ~~means~~ for receiving said serial bit stream and outputting said frames in a consecutive order, said shift register ~~means~~ including a serial input portion and a parallel output portion and having at least as many stages as the number of bits of a frame,
first clock circuitry that generates first clock pulses, separated by a first time period, for clocking the serial input portion of the shift register;
second clock circuitry that generates second clock pulses for clocking the parallel output portion of the shift register, the second clock circuitry generating the second clock pulses responsive to the first clock pulses, and
~~characterized by control circuitry~~ ling means for detecting whether or not a frameheader is present at the output of said parallel output portion and, if not, controlling said shift register ~~means~~ so that the clocking of the outputting of a frame ~~from said parallel output portion~~ is delayed by at least ~~one~~ the first time period ~~which is needed for shifting a bit in said serial input portion from a stage to a next one, until synchronization is reached, the control circuitry delaying the clocking of the parallel output portion by preventing one of the first clock pulses from reaching the second clock circuitry.~~
outputting of a frame is repeated ~~several times~~ until synchronization is reached.
2. (Currently Amended) The device according to claim 1, wherein said control ~~circuitry~~ ling means is adapted so that ~~the delay of the preventing of one of the first clock pulses from reaching the second clock circuitry~~ outputting of a frame is repeated ~~several times~~ until synchronization is reached.

3. (Previously Presented) The device according to claim 1, wherein the frames have a fixed length.
4. (Original) The device according to claim 3, wherein the frames are bytes.
5. (Currently Amended) The device according to claim 1, ~~comprising a first clock means for generating first clock pulses clocking said parallel output portion of said shift register means,~~ wherein the control circuitry is ~~ling means~~ are adapted to control said ~~first~~ second clock circuitry means so that said ~~first~~ second clock pulses are delayed by at least ~~one~~ the first time period which is needed for shifting a bit in said serial input portion from a stage to a next ~~stage one~~.
6. (Currently Amended) The device according to claim 5, wherein each frame includes N bits, ~~and the second clock circuitry means is provided for generating second clock pulses for clocking said serial input portion of said shift register means, and said first clock means converts said second~~ first clock pulses into said ~~first~~ second clock pulses, ~~the second clock pulses separated by having a second time period which that is N times longer than the first time period of said second~~ first clock pulses, ~~characterized in that and wherein said control circuitry ling means is adapted to control said first second clock circuitry means so that said first second clock pulses are delayed by at least one the first time period of said second first clock pulses.~~
7. (Currently Amended) The device according to claim 5, wherein said control circuitry ling means is adapted to supply a ("~~kick pin~~") control signal to said ~~first~~ second clock circuitry means to prevent the one of the first clock pulses from reaching the second clock circuitry, and said ~~first~~ second clock circuitry means is adapted so that ~~it~~ the one of the first clock pulses is blocked by said control signal for at least ~~one~~ the first time period which is needed for shifting a bit in said serial input portion of said shift register ~~means~~ from a stage to a next ~~stage one~~.

8. (Currently Amended) A frame synchronizing method for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, the method comprising the steps of:

inputting said serial bit stream into a serial input portion of a serial input parallel output shift register ~~means~~ having at least as many stages as the number of bits of a frame, and

generating first clock pulses, by first clock circuitry, for clocking the serial portion of the shift registers, the first clock pluses separated by a first time period

generating second clock pulses, by second clock circuitry, for clocking a parallel output portion of the shift register, the second clock pulses derived from the first clock pulses,

outputting said frames in a consecutive order from a the parallel output portion of said shift register ~~means, characterized by the further steps of:~~

detecting whether or not a frameheader is present in the output of said parallel output portion, and,

if not, delaying the generation of the second clock pulses ~~outputting of a frame from said parallel output portion~~ by at least ~~one~~ the first time period by preventing one of the first clock pulses from reaching the second clock circuitry which is needed for shifting a bit in said serial input portion from a stage to a next one, until synchynchronization is reached.

9. (Currently Amended) The method according to claim 8, wherein ~~the step of~~ delaying the preventing of one of the first clock pulses from reaching the second clock circuitry ~~outputting of a frame~~ is repeated several times until synchronization is reached.

10. (Previously Presented) The method according to claim 8, wherein the frames have a fixed length.

11. (Original) The method according to claim 10, wherein the frames are bytes.

12. (Currently Amended) The method according to claim 8, ~~comprising the further step of generating first clock pulses clocking the outputting of the frames from said parallel output portion of said shift register means, characterized in that said first~~ the second clock pulses are delayed by at least ~~one~~ the first time period which is needed for shifting a bit in said serial input portion from a stage to a next stage one.

13. (Currently Amended) The method according to claim 12, comprising the further steps of: ~~generating second clock pulses for clocking the inputting of said serial bit stream into said serial input portion of said shift register means, and converting said second~~ first clock pulses into said ~~first~~ second clock pulses, the second clock pulses having separated by a second time period which that is N times longer than the first time period of said ~~second~~ first clock pulses, wherein each frame includes N bits, and characterized in that said first second clock pulses are delayed by at least one the first time period of said second first clock pulses.

14. (Currently Amended) The method according to claim 12, ~~characterized by the further steps of:~~ further comprising generating a ("kick-pin") control signal[[,]] if a frameheader is not detected in the output of said parallel output portion of said shift register means, and blocking the generation of said ~~first~~ second clock pulses by said control signal for at least ~~one~~ the first time period which is needed for shifting a bit in said serial input portion of said shift register means from a stage to a next stage one.

15. (Previously presented) A digital data transmission systems like SONET/SDH or Gigabit Ethernet comprising a device as claimed in claim 1 where serial data are transported over a single channel and, at the receiving side, is converted into parallel data for further processing.